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AN10753

ESD protection for USB 2.0 interfaces

Rev. 3 — 5 February 2013 **Application note**

Document information

Info	Content
Keywords	ESD, USB, PESD5V0X1BL, PESD12VS1UL, PRTR5V0U2F, PRTR5V0U2K
Abstract	This application note describes how to protect USB 2.0 ports with NXP general-application discretes parts, i.e. low-capacitance ElectroStatic Discharge (ESD) protection diodes PESD5V0X1BL, PRTR5V0U2F and PRTR5V0U2K.

Revision history

Rev	Date	Description
3	20130205	Section 6 “Appendix” added.
2	20101101	Measurement results for PRTR5V0U2F and PRTR5V0U2K added. Table 2 “Device ESD failure threshold classification according to MIL-STD 883” added.
1	20090115	Initial version

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1. Introduction

An Integrated Circuit (IC) connected to external ports can be damaged by ElectroStatic Discharge (ESD) from the operating environment.

The result of ever-shrinking IC process technology is the decrease of ESD robustness because of the smaller geometry of the silicon die.

Traditional methods to prevent ICs from ESD damage are the implementation of additional devices such as:

- Zener diodes
- Varistors
- Transient Voltage Suppressor (TVS) diodes
- Bipolar clamp diodes

However, at much higher data rates, the parasitic characteristics can distort or deteriorate signal integrity. This application note examines the general parameters the hardware designer should look at to increase the ESD robustness of the application, e.g. USB interfaces.

2. ElectroStatic Discharge (ESD) basics

ESD events are one of the most challenging issues in the semiconductor industry these days due to ever-shrinking IC structures of semiconductor devices.

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Fig 1. Typical attention sign

The smaller the geometry of the silicon die, the more ESD sensitive are the ICs, and the more IC area is required for the ESD protection of the device (see Figure 2).

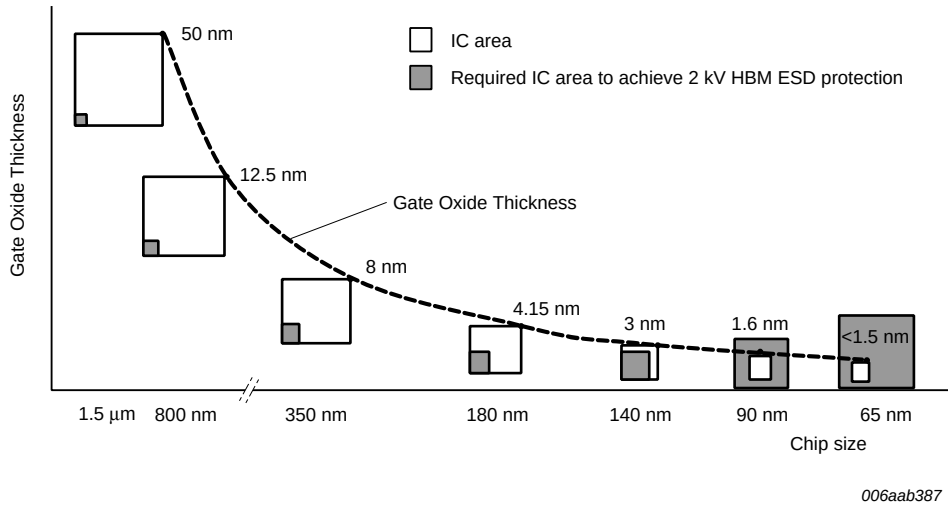

Fig 2. Required IC area as a function of chip size; typical values

An ESD event is the transfer of energy between two bodies of different electrostatic potential.

ElectroStatic Discharge can happen by contact, or via an ionized ambient discharge.

There are several models known:

- Human Body Model (HBM) - A human body is discharged to an electronic component.
- Machine Model (MM) - A machine or tool is discharged to an electronic component.
- Charged Device Model (CDM) - An electronic component is discharged to the ambient.
- System Level (IEC) - A human body is discharged to a powered system.

This application note covers the difference between the Human Body Model and the System Level Model which are both Human Body Models, but the System Level Model is relevant for a complete solution, e.g. a portable multimedia device.

2.1 Human Body Model (HBM) - Standards IEC/EN 61340-3-1 or MIL-STD 883

This standard covers the manual handling of none-powered electronic components. The handling can be picking up a device for testing or mounting the device on a Printed-Circuit Board (PCB)!

A capacitor of 100 pF is charged and then discharged via a 1.5 kΩ resistor to the Device Under Test (DUT).

The waveform of IEC 61340-3-1 is shown in Figure 3, the rise time is defined up to 10 ns.

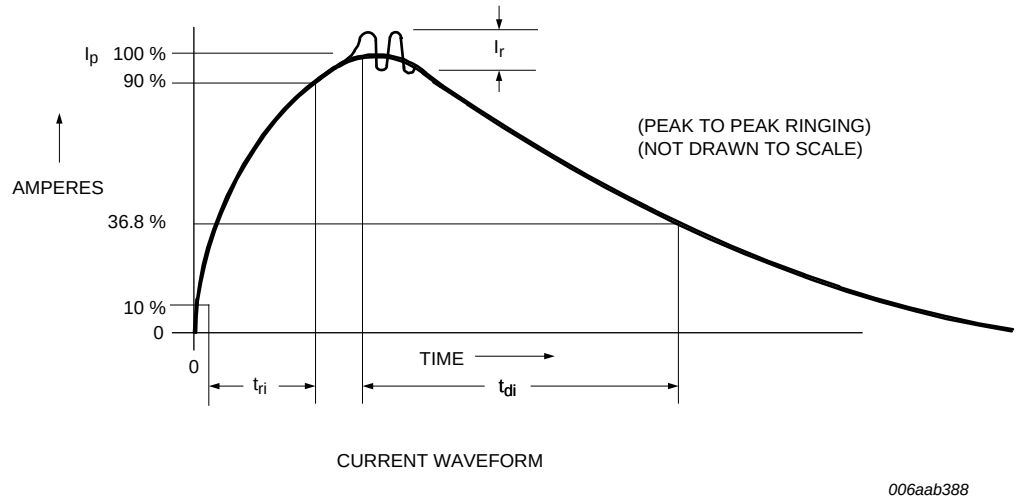

Fig 3. MIL-STD 883 waveform

Table 1. Waveform parameters according to MIL-STD 883

Step	Test voltage (kV)	Peak current (A)
1	0.5	0.33
2	1	0.67
3	2	1.33
4	4	2.67

Table 2. Device ESD failure threshold classification according to MIL-STD 883

Class	Threshold voltage (V)
0	< 250
1A	250 to 499
1B	500 to 999
1C	1000 to 1999
2	2000 to 3999
3A	4000 to 7999
3B	≥ 8000

2.2 System Level (IEC) - Standard IEC 61000-4-2

This standard covers the manual handling of a powered electronic system, e.g. touching an interface connector.

A capacitor of 150 pF is charged and then discharged via a 330 Ω resistor to the DUT.

The waveform of IEC 61000-4-2 is shown in Figure 4, the rise time is defined between 0.7 ns and 1 ns.

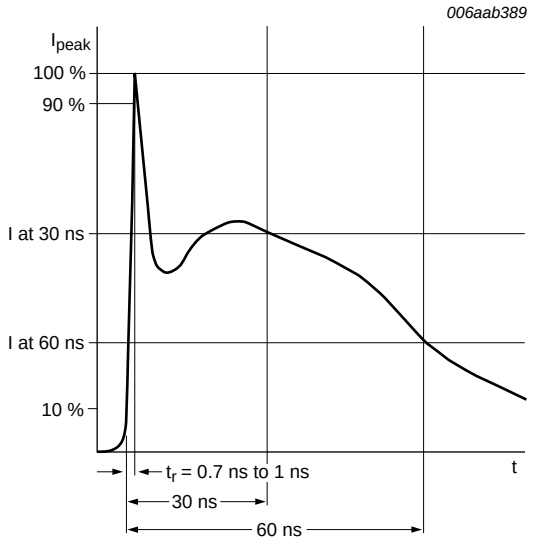

Fig 4. IEC 61000-4-2 waveform

There are different levels for test proposals mentioned.

For contact or air discharge test, they differ in the voltage values (see Table 3).

Table 3. Waveform parameters according to IEC 61000-4-2

Level	Test voltage (kV)		Current (A)		
	Contact	Air	Peak current	After 30 ns	After 60 ns
1	2	2	7.5	4	2
2	4	4	15	8	4
3	6	8	22.5	12	6
4	8	15	30	16	8

2.3 Standard comparison

Both models differentiate concerning the test voltages.

One can see that a 2 kV discharge voltage refers to different discharge currents.

Therefore, NXP recommends external ESD protection to be compliant with the IEC 61000-4-2 standard.

3. USB interface protection

The USB 2.0 standard covers several data transmission rates. It is also compliant to the former specification USB 1.1.

Following data transmission rates are covered:

- 1.5 MBit/s (low speed)
- 12.0 MBit/s (full speed)
- 480 MBit/s (hi-speed)

For the hi-speed mode, the maximum allowed capacitance according to the USB 2.0 specification is 10 pF overall.

These 10 pF are shared by a maximum of 5 pF for the transceiver itself, and the other 5 pF for the connector, PCB traces, and additional components.

Figure 5 shows the maximum allowable line capacitance at different data speeds.

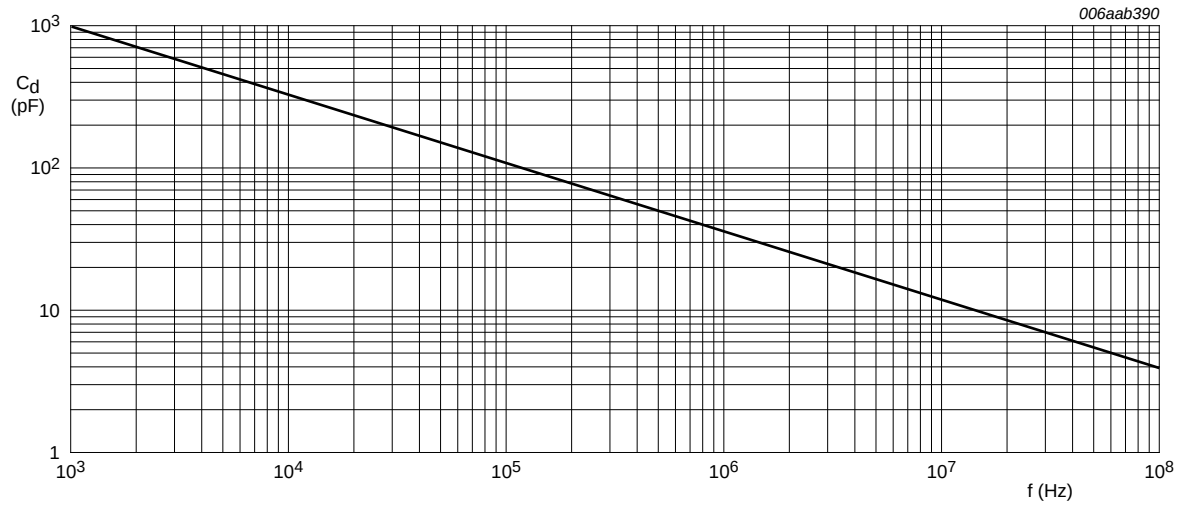

Fig 5. Line capacitance as a function of line frequency; typical values

To expose any issue in USB data lines, the measurement method “eye pattern”, also known as “eye diagram”, is used.

It represents a digital signal that provides minimum and maximum voltage levels and signal jitter.

One can also measure the signal rise time and the fall time, as well as overshoot and undershoot.

Line capacitance and bandwidth effects of the USB data transmission can be evaluated!

USB 2.0 signal mask specifications are provided by the USB Implementers Forum.

Figure 6 shows an “eye pattern” with the critical issues of a USB 2.0 data signal.

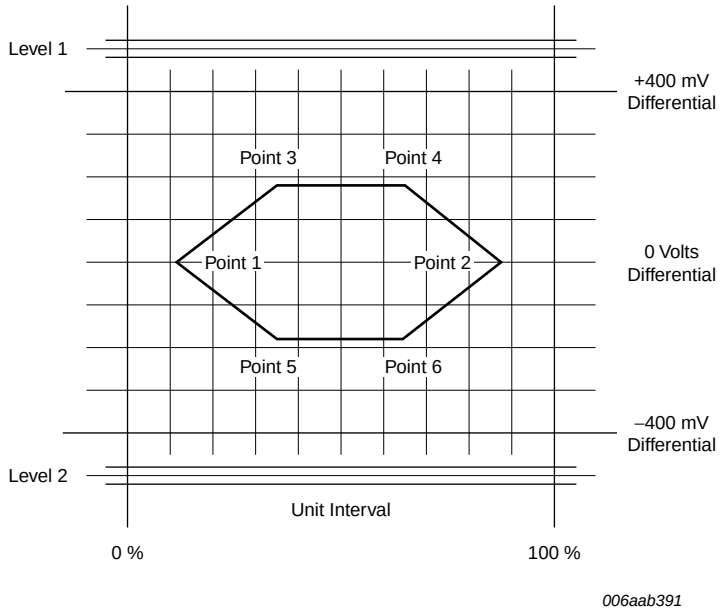

Fig 6. USB 2.0 “eye pattern”

3.1 Component differences

The NXP product portfolio offers two different approaches:

One component for each single line to be protected:

- Single-line protection for D+ and D– bidirectional configuration (PESD5V0X1BL).
- Single-line protection for V_{BUS} unidirectional configuration (PESD12VS1UL).

One package for complete USB interface protection:

- Dual line protection in rail-to-rail configuration, i. e. D+, D– and V_{BUS} (PRTR5V0U2x).

4. Measurement methods

4.1 USB 2.0 protection with PESD5V0X1BL

To evaluate the PESD5V0X1BL behavior in USB 2.0 applications, a reference board (see Figure 7) was designed.

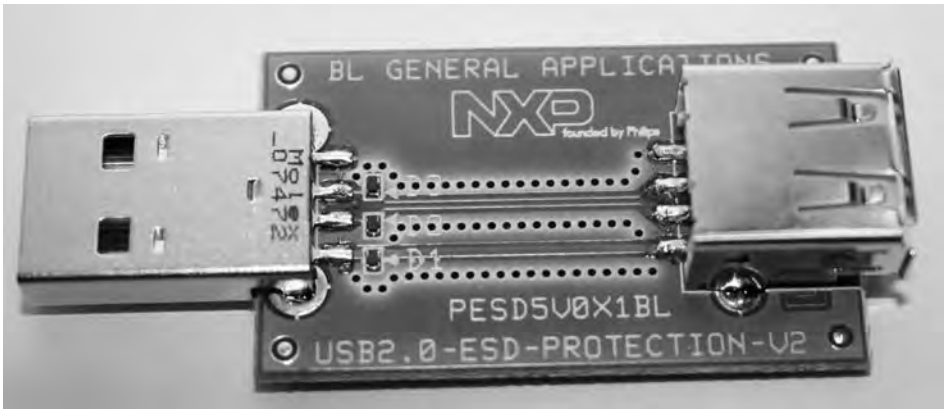

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Fig 7. USB 2.0-ESD-Protection-V2-board

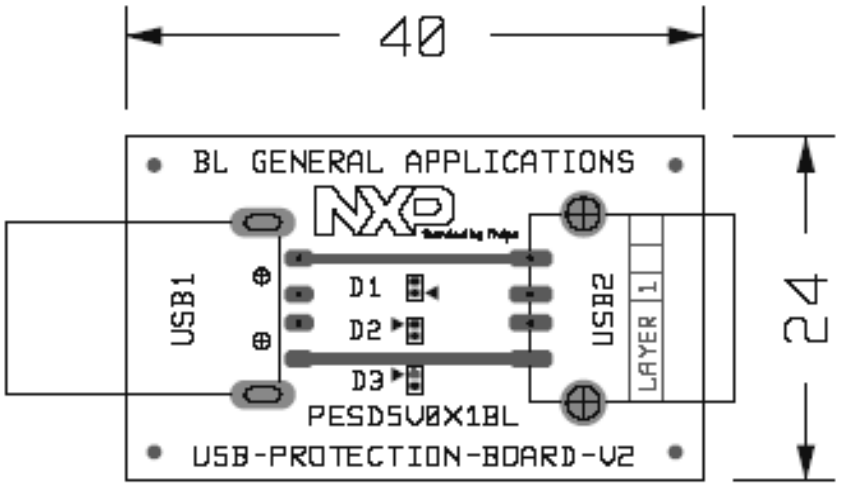

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Fig 8. USB 2.0-ESD-Protection-V2-assembly diagram

An image of the PCB layer structure having two controlled impedance lines is shown in Figure 9.

Figure 10 provides the schematic of the demo board using PESD5V0X1BL for D1 and D2 each. In order to meet the USB charging requirements of even more than 5 V, there was a PESD12VS1UL chosen for D3.

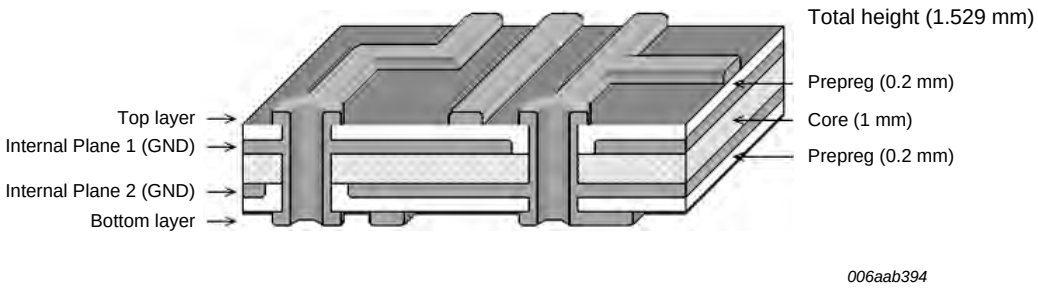

Fig 9. USB 2.0 PCB layer structure

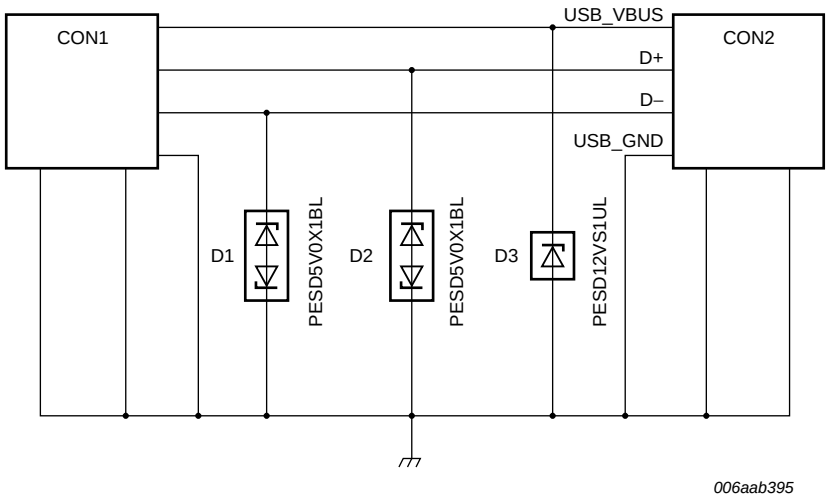

Fig 10. USB 2.0 ESD-Protection-V2-schematic

4.1.1 Reference measurements

To evaluate the influence of different ESD protection components, the measurements were done in several steps.

A board without a device was evaluated as reference.

Comparing all “eye patterns” demonstrates the degradation caused by the ESD protection devices.

The first test was done without any protection diode (see Figure 11), the result pattern is shown in Figure 13.

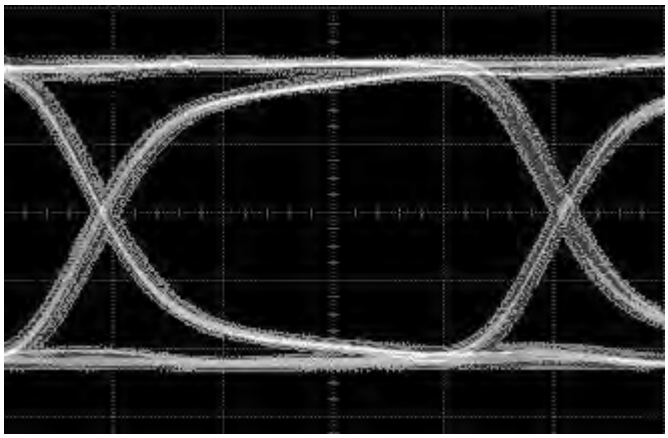

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Fig 11. USB 2.0 “eye pattern” without DUT

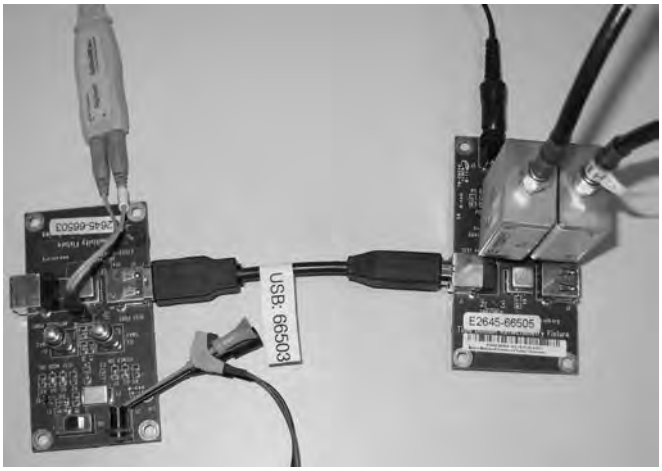

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Fig 12. Test setup for USB 2.0 “eye pattern” without DUT

4.1.2 DUT measurements

DUT measurements done on three different PCBs using two different PESD5V0X1BL diodes each are shown below.

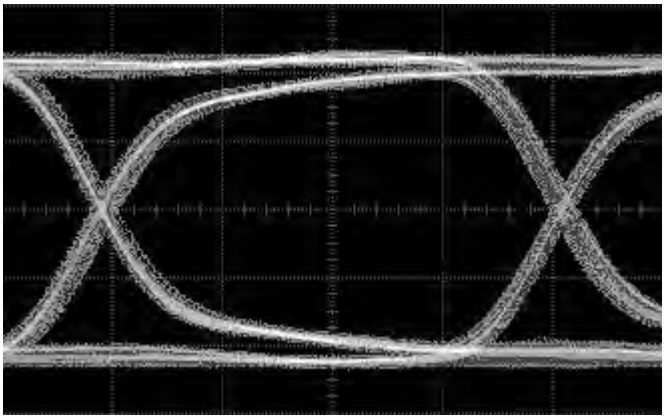

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Fig 13. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB1

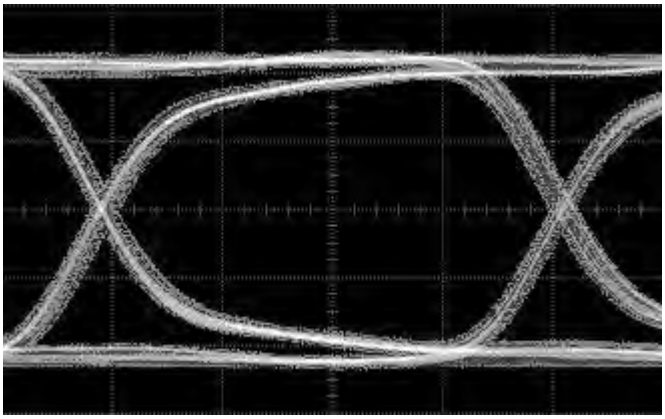

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Fig 14. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB2

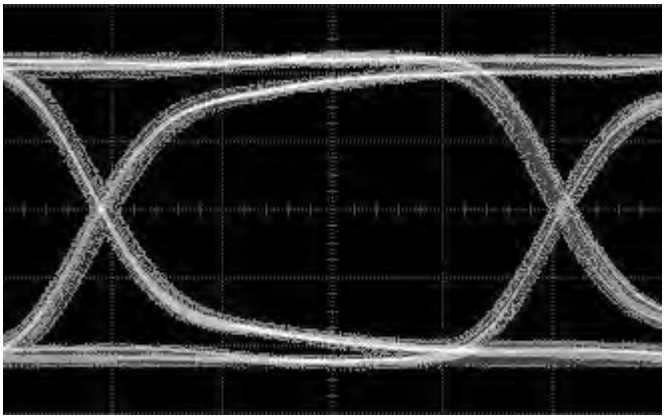

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Fig 15. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB3

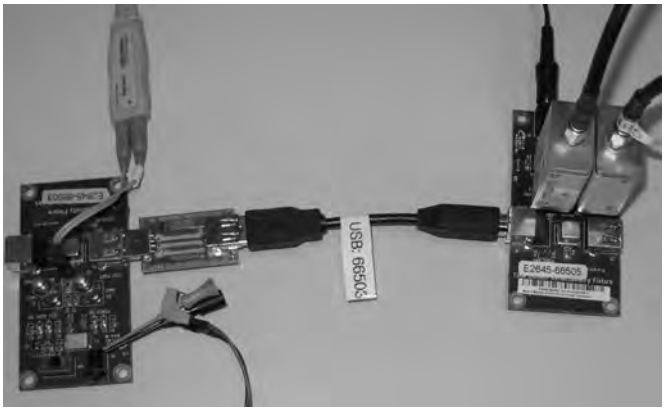

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Fig 16. Test setup for USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode

4.2 USB 2.0 protection with PRTR5V0U2F/K

In order to evaluate the PRTR5V0U2F/K behaviors in USB 2.0 applications, two reference boards were designed (see Figure 17 and Figure 18).

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Fig 17. USB 2.0 ESD-Protection-V3-board

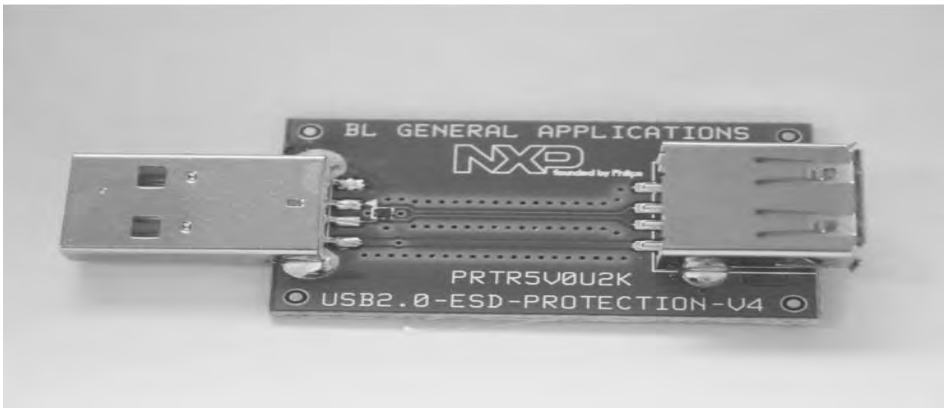

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Fig 18. USB 2.0 ESD-Protection-V4-board

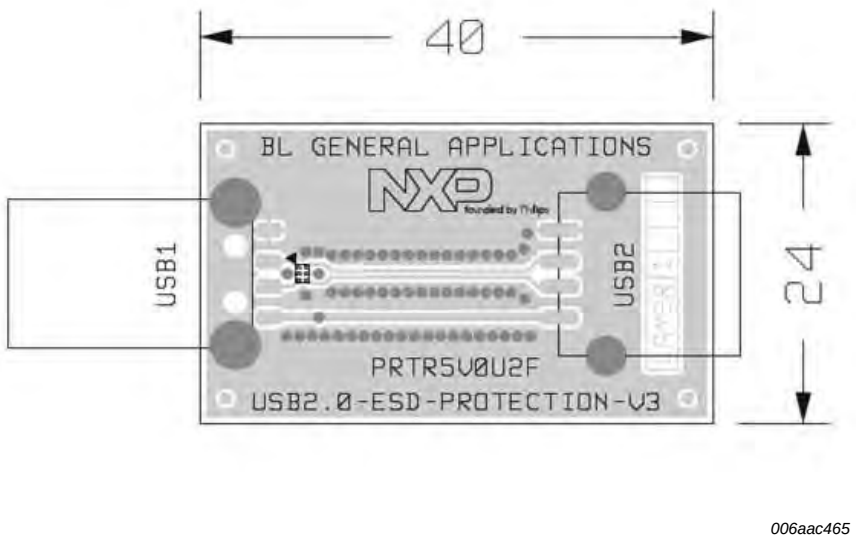

Fig 19. USB 2.0-ESD-Protection-V3/V4-assembly diagram

The PCB layer structure for the USB 2.0-ESD-Protection-V3/V4-assembly diagram as shown in Figure 19 is similar to the USB 2.0-ESD-Protection-V2-board (see Figure 9).

Figure 20 provides the schematic of both, V3 and V4 reference boards, with only slight differences with respect to the packages. PRTR5V0U2F is housed in an SOT886 package of dimensions 1.45 × 1 × 0.5 mm, and PRTR5V0U2K is housed in an SOT891 package of dimensions 1 × 1 × 0.5 mm.

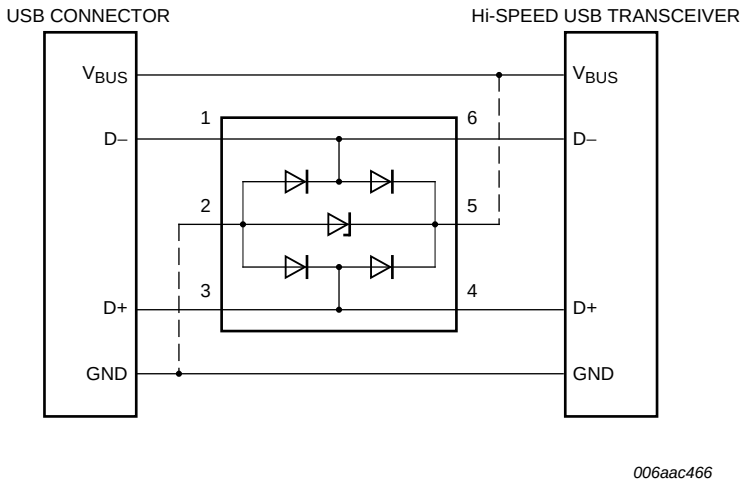

Fig 20. USB 2.0-ESD-Protection-V3/V4-schematic

4.2.1 Reference measurements

To evaluate the influence of different ESD protection components, the measurements were done in several steps.

A board without a device was evaluated as reference.

Comparing all “eye patterns” demonstrates the degradation caused by the ESD protection devices.

The first test was done without any protection diode (see Figure 21) using a similar test setup to Figure 12.

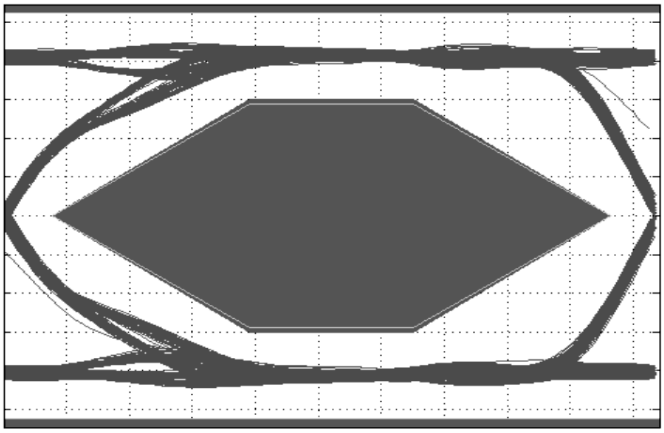

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Fig 21. USB 2.0 “eye pattern” without DUT

4.2.2 DUT measurements

The DUT measurements were done on three different PCBs using PRTR5V0U2F and PRTR5V0U2K on a similar test setup to Figure 16.

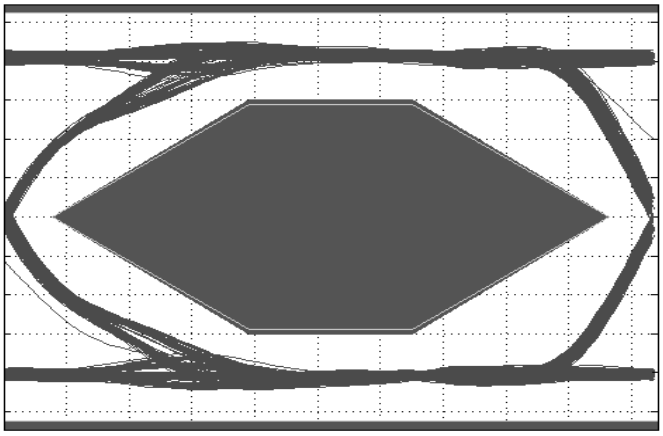

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Fig 22. USB 2.0 “eye pattern” with PRTR5V0U2F protection diode; PCB1

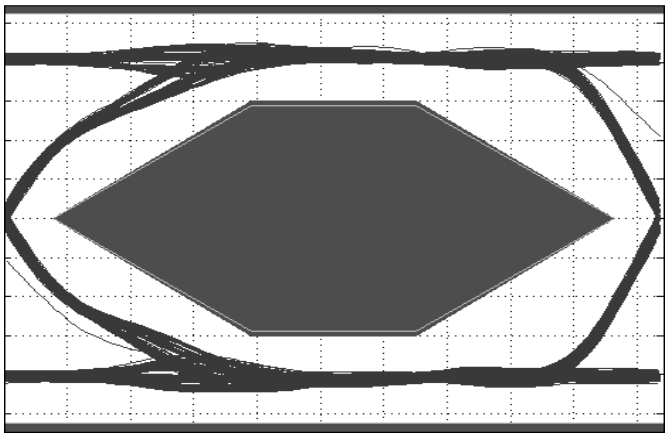

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Fig 23. USB 2.0 “eye pattern” with PRTR5V0U2F protection diode; PCB2

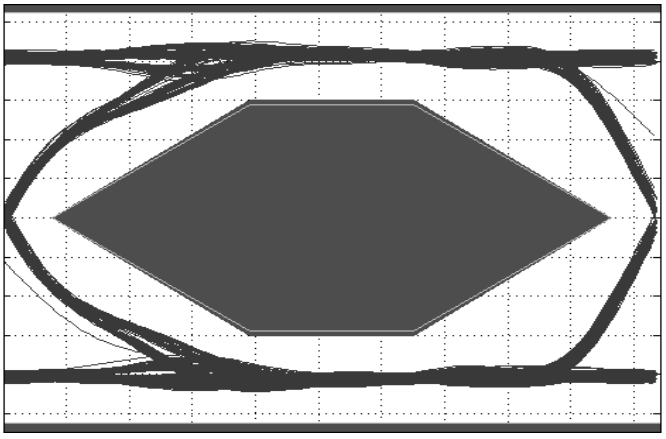

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Fig 24. USB 2.0 “eye pattern” with PRTR5V0U2F protection diode; PCB3

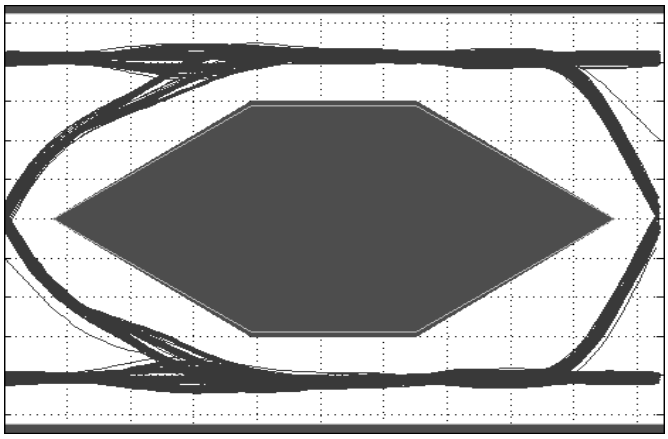

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Fig 25. USB 2.0 “eye pattern” with PRTR5V0U2K protection diode; PCB1

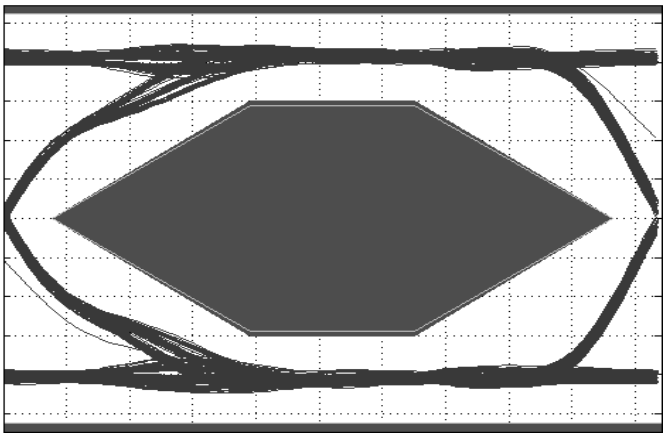

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Fig 26. USB 2.0 “eye pattern” with PRTR5V0U2K protection diode; PCB2

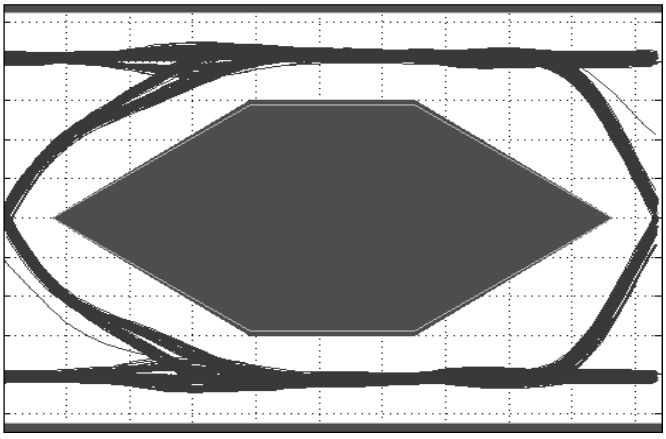

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Fig 27. USB 2.0 “eye pattern” with PRTR5V0U2K protection diode; PCB3

5. Summary

The NXP low-capacitance ESD protection devices offer best results for USB 2.0 hi-speed applications.

The “eye pattern” evaluations show that NXP’s low-capacitance ESD protection devices have an extremely low impact on the USB 2.0 data signals.

This option gives the hardware designer some space for additional capacitance on the USB 2.0 signal lines!

6. Appendix

6.1 USB 2.0 ESD protection portfolio

Table 4. USB 2.0 ESD protection portfolio

Type number	C_{line} [1]	$V_{BUS(max)}$	ESD rating	Package	AEC-Q101
PRTR5V0U2X	1.0 pF	5.0 V	8 kV	SOT143B	YES
PRTR5V0U2AX	1.8 pF	5.0 V	8 kV	SOT143B	YES
PRTR5V0U4D	1.0 pF	5.0 V	8 kV	SOT457	YES
PRTR5V0U2F	1.0 pF	5.0 V	8 kV	DFN1410-6	NO
PRTR5V0U2K	1.0 pF	5.0 V	8 kV	DFN1010-6	NO
PUSBM5V5X4-TL	1.0 pF	5.5 V	8 kV	DFN1616-6	NO
PUSBM12VX4-TL	1.0 pF	12 V	8 kV	DFN1616-6	NO
PUSBM15VX4-TL	1.0 pF	15 V	8 kV	DFN1616-6	NO
PUSBM30VX4-TL	1.0 pF	30 V	8 kV	DFN1616-6	NO
IP4369CX4	0.8 pF	only D– lines	8 kV	WLCSP4	NO

[1] Data lines (D+/D–)

6.2 USB 3.0 ESD protection portfolio

Table 5. USB 3.0 ESD protection portfolio

Type number	C_{line}	$V_{BUS(max)}$	ESD rating	Package	AEC-Q101
IP4294CZ10-TBR	0.50 pF	only D– lines	10 kV	DFN2510A-10	NO
IP4292CZ10-TBR	0.55 pF	only D– lines	8 kV	DFN2510A-10	NO

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